In the Claims:

1. (Currently Amended) A method of patterning metal layers of a semiconductor wafer, the method comprising:

depositing a first conductive layer over a substrate;

depositing an insulating layer over the first conductive layer;

depositing a second conductive layer over the insulating layer;

depositing a first layer of resist over the second conductive layer;

patterning the first layer of resist with a first pattern;

developing said patterned first layer of resist;

removing portions of said first layer of resist according to said first pattern to expose portions of said second conductive layer;

depositing a second layer of resist over remaining portions of the first layer of resist and exposed portions of said second conductive layer;

patterning the second layer of resist with a second pattern; ~~and~~

developing said patterned second layer of resist;

stripping portions of said second layer of resist according to said second pattern; and

~~simultaneously transferring~~ etching the first ~~pattern to the first~~ conductive layer according to the first pattern and the ~~second pattern to the~~ second conductive layer according to the second pattern in a single etching process.

2. (Currently Amended) The method according to Claim 1 wherein the single etching process ~~transferring the first and second patterns comprise~~ comprises exposing the wafer to a single reactive ion etch process.

3. (Original) The method according to Claim 1 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

4. (Original) The method according to Claim 1 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

5. (Currently Amended) The method according to Claim 1 wherein the insulating layer comprises a capacitor dielectric, wherein etching ~~transferring the first pattern to~~ the first conductive layer comprises forming bottom metal plates of a MIM capacitor, and wherein etching ~~transferring the second pattern to~~ the second conductive layer comprises forming top metal plates of the MIM capacitor.

6. (Currently Amended) The method according to Claim 1 further comprising etching ~~transferring the first pattern to~~ the insulating layer according to the first pattern.

7. (Currently Amended) A method of patterning metal layers of a semiconductor wafer, the wafer comprising a first conductive layer, an insulating layer disposed over the first conductive layer and a second conductive layer disposed over the insulating layer, the method comprising:

depositing a first layer of resist over the second conductive layer;

patterning the first layer of resist with a first pattern;

developing said patterned first layer of resist;

removing portions of said first layer of resist according to said first pattern to expose portions of said second conductive layer;

depositing a second layer of resist over remaining portions of the first layer of resist and exposed portions of said second conductive layer;

patterning the second layer of resist with a second pattern;

developing said patterned second layer of resist;

stripping portions of said second layer of resist according to said second pattern; and

~~simultaneously transferring~~ etching the first ~~pattern to the first~~ conductive layer according to the first pattern and ~~transferring the second pattern to~~ the second conductive layer according to the second pattern in a single etching process.

8. (Currently Amended) The method according to Claim 7 wherein the single etching process ~~transferring the first and second patterns comprise~~ comprises exposing the wafer to a reactive ion etch process.

9. (Original) The method according to Claim 8 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

10. (Original) The method according to Claim 8 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

11. (Currently Amended) The method according to Claim 8 wherein the insulating layer comprises a capacitor dielectric, wherein etching ~~transferring the first pattern to the~~ first

conductive layer comprises forming bottom metal plates of a MIM capacitor, and wherein etching ~~transferring the second pattern to~~ the second conductive layer comprises forming top metal plates of the MIM capacitor.

12. (Currently Amended) The method according to Claim 7 further comprising etching ~~transferring the first pattern to~~ the insulating layer according to the first pattern.

13. (Currently Amended) A method of forming capacitive plates of a MIM capacitor, comprising:

providing a wafer having a substrate;

depositing a first conductive layer on the substrate;

depositing a capacitor dielectric layer over the first conductive layer;

depositing a second conductive layer over the capacitor dielectric layer;

depositing a first layer of resist over the second conductive layer;

patterning the first layer of resist with a first pattern;

developing said patterned first layer of resist;

removing portions of said first layer of resist according to said first pattern to expose portions of said second conductive layer;

depositing a second layer of resist over remaining portions of the first layer of resist and exposed portions of said second conductive layer;

patterning the second resist with a second pattern; ~~and~~

developing said patterned second layer of resist;

stripping portions of said second layer of resist according to said second pattern; and

~~simultaneously transferring the first pattern to~~ etching the first conductive layer according to the first pattern and ~~transferring the second pattern to~~ the second conductive layer according to the second pattern in a single etching process.

14. (Currently Amended) The method according to Claim 13 wherein the single etching process ~~transferring the first and second patterns comprise~~ comprises exposing the wafer to a reactive ion etch process.

15. (Original) The method according to Claim 13 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

16. (Original) The method according to Claim 13 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

17. (Currently Amended) The method according to Claim 13 further comprising etching ~~transferring the first pattern to~~ the insulating layer according to the first portion.

18. (New) The method according to Claim 1 wherein said step of patterning the first layer of resist comprises the step of patterning with a lithographic process.

19. (New) The method according to Claim 18 wherein said step of patterning the second layer of resist comprises the step of patterning with a lithographic process.